IN THE UNI TED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Helmut Theiler	Art Unit	: 2836
Serial No.	: 10/521,931	Examiner	: Adi Amrany
Filed	: July 19, 2005	Conf. No.	: 2109
Title	: CIRCUIT ARRAY		

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicants submit this request under the Pre-Appeal Conference Pilot Program described in the OG Notice dated July 12, 2005 and extended until further notice as of January 10, 2006. This request is being filed with a Notice of Appeal. Review of the matters identified below is requested because the rejections of record are clearly not proper and are without basis, in view of a clear legal or factual deficiency in the rejections.

Claims 1-11 and 19-22 are pending, of which claims 1 and 6 are independent.

Claims 6, 9 and 11 were rejected under 35 U.S.C. §102(b) as being anticipated by Peil (US 4,560,909) and claims 1-11 and 19-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dalnodar. Applicants have addressed many of these rejections in reply dated October 22, 2009, but the rejections were maintained in a Final Office Action dated November 19, 2008.

Accordingly, Applicants ask that the panel review the issues below, which Applicants submit will dispose of the entire appeal. Applicants reserve the right to expand these issues and/or present new issues should they subsequently file an appeal brief.

I. Claim 1 —Multiple features are missing from Dalnodar.

Claim 1 was rejected as being unpatentable over Dalnodar (US 5,504,400). Claim 1 recites, among other limitations, "a logic unit to generate the switch control signal based on one or more logical load control signals and the logical detection signal." Dalnodar fails to disclose or suggest such a logic unit for at least two reasons.

First, claim 1 requires that the switch control signal be generated by the logic unit based on at least two signals, namely "one or more logical load control signals and the logical detection

signal." In the current rejection, the examiner compares Dalnodar's diac (DC1) to the claimed logic unit. However, a diac (such as Dalnodar's DC1) is a two terminal device that allows current to flow when a voltage across the two terminals is greater than a breakdown voltage of the device. As shown in Fig. 4 of Dalnodar (reproduced below), the diac DC1 includes a single input (the voltage, v_c, at the node above C1) and a single output (the voltage supplied to the gate 17 of triac T1).

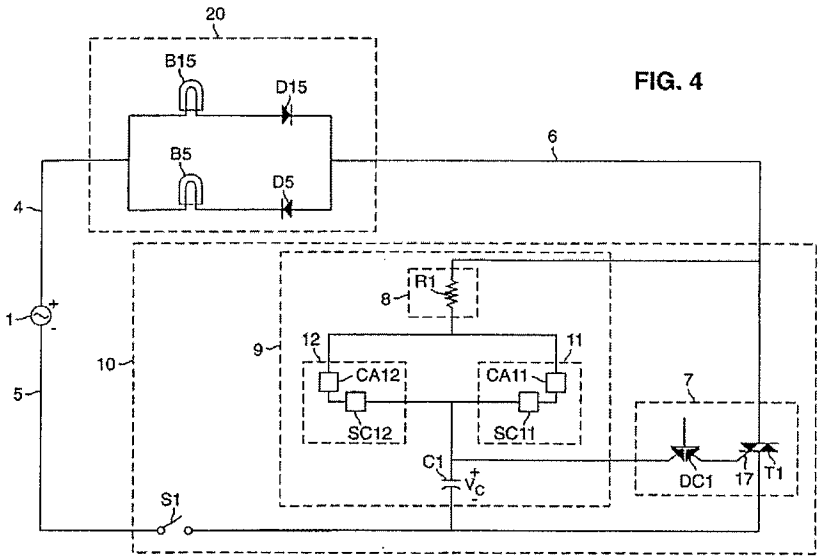

FIG. 4

Regarding the functionality of the diac (DC1) and the triac (T1), Dalnodar states:

> The triac T1 may be triggered into conduction during each half cycle if the voltage v_c across the capacitor C1 is sufficiently high such that the diac DC1 breaks down and partially discharges the capacitor into the gate 17 of triac T1.[1]

As such, in Dalnodar, only a single input is provided to the diac DC1, namely, the voltage across capacitor C1. Thus, the output signal (17) generated by Dalnodar's diac is not "based on one or more logical load control signals and the logical detection signal" as recited in the Applicants' claim 1.

Further, claim 1 requires that the logical unit generate the switch control signal based on "one or more logical load control signals and the logical detection signal." In contrast, to the claimed logical load control signals and logical detection signal, Dalnodar discloses an analog signal. In this regard, the examiner states "Dalnodar discloses that analog signals are passed

[1] Dalnodar, col. 5, lines 52-55.

from the phase detectors (11, 12) to the diac (DC1)."[2] The analog signal which provides the input to Dalnodar's diac DC1 is the voltage across capacitor C1 (an analog voltage) which is generated based on the values of potentiometers VR11 and VR12. In this regard, Dalnodar states:

> Current will therefore flow through the potentiometer VR11 and the resistance of the potentiometer VR11 will control the charge rate of the capacitor C1. If the potentiometer VR11 is set to its maximum value, then the current charging the capacitor will be at its minimum value. As a result, the voltage v_c will be insufficient to break down the diac DC1, and the triac T1 will not be switched into conduction. As the resistance setting of the potentiometer VR11 is reduced, a larger current will flow... causing capacitor C1 to charge faster such that the voltage v_c will become sufficient to break down the diac DC1 at some point late in the half cycle.[3]

Dalnodar further states:

> This implies that voltage v_c will be non zero at the end of the half cycle. Furthermore, if the voltage v_c was not sufficient to break down the diac DC1 than the capacitor C1 will not have partially discharged, and the voltage at the end of the half cycle may be any value less than the break down voltage of the diac DC1.

As such, in contrast to the Applicants' claimed logical signals, in Dalnodar the load control signal delivered by the capacitor C1 to diac DC1 is analog. Therefore, Applicants request the rejection of claim 1 be withdrawn.

II. Claim 22 —Multiple features are missing from Dalnodar.

Claim 22 depends from claim 1 and is patentable for at least the reasons described above in relation to claim 1. Claim 22 adds additional limitations regarding the "logical control signal" of claim 1 and recites "wherein the logical load control signal comprises a signal selected from a group consisting of a logical 0 and a logical 1."

Dalnodar fails to disclose or suggest such a logical load control signal. In contrast, to the claimed logical load control signals comprising either a logical 0 and a logical 1, Dalnodar discloses an analog signal (see discussion above in relation to claim 1). The examiner acknowledges that the signal supplied to DC1 is an analog signal and states "Dalnodar discloses

[2] Office Action, page 5.
[3] Dalnodar, col. 5 line 65 - col. 6, line 9.

that analog signals are passed from the phase detectors (11, 12) to the diac (DC1)."[4] However, in rejecting claim 22, the examiner states "Dalnodar discloses the diac provides a logical 0 and a logical 1 to cause the triac to switch... The diac would output a 0 and 1 regardless of where it is placed in the circuit (as the DAC connected to the output of the phase detectors or as the switch control for the triac)."[5]

To the best of the Applicants' understanding, the examiner appears to suggest that it would have been obvious to add two additional diacs to Dalnodar's circuit between the variable resistors VR11 and VR12 and the capacitor C1. However, inserting diacs in such a location would no longer allow Dalnodar's circuit to function appropriately because the capacitor C1 would no longer be charged in the same manner. Rather, if such diacs were added, the capacitor would only be charged when the voltage across the resistor VR11 or VR12 exceeded the breakdown voltage of the diac (see discussion above re charging/discharging of capacitor C1).

As such, it would not have been obvious to place additional diacs in Dalnodar's circuit and the Applicants, therefore, request that the rejection of claim 22 be withdrawn.

III. Claim 6 —Multiple features are missing from Peil.

Claim 6 recites an electronic device that includes "a circuit array for controlling a switch to apply voltage to first and second loads based on whether a phase of the AC voltage is positive or negative and logical load control signals generated separately for the first and second loads." In contrast, Peil discloses "a manually adjustable phase shift network including the manually variable resistor 20, and a capacitor 21." (Peil, col. 4 lines 4-6). Describing the function of the phase shift network Peil states:

> The output of the phase shift network available at the interconnected terminals of 20 and 21 is coupled via the diac 19 to the triac 18, as earlier noted. The diac is bidirectionally conductive, breaking down in either direction, when a predetermined breakdown voltage is exceeded. Assuming that the voltage produced in the phase shift network momentarily exceeds that required to break down the diac, a trigger voltage will be coupled to the triac causing it to conduct as some point in the ac wave. Conduction by the diac 19 partially discharges the capacitor 21 into the gate of the triac 18.[6]

---

[4] Office Action, page 5.
[5] Office Action, page 9.
[6] Peil, col. 5 lines 27-38.

In contrast to the Applicants' claimed logical signals, in Peil the load control signal is delivered by a manually variable resistor and is therefore an analog signal. Therefore, Applicants request that the 35 U.S.C. 102(b) rejection of claim 6 be withdrawn.

IV. Dependent Claims

Claims 2-5 and 19-22 depend from claim 1 and claims 7-11 depend from claim 6. Claims 2-5, 7-11, and 19-22 and should be allowed for at least the same reasons as the claims on which they depend. Applicants reserve the right to point out deficiencies in the Examiner's analysis regarding each of the dependent claims.

V. Conclusion

In view of the above, all of the claims are believed to be in condition for allowance. A formal notice of allowance is thus respectfully requested.

This request is filed with a Notice of Appeal. The fees for the Notice of Appeal are being paid herewith by way of Deposit Account No. 06-1050. Please apply any other charges or credits to Deposit Account No. 06-1050, Referencing Attorney Docket No. 14603-0009US1.

Respectfully submitted,

Date: 1/6/09

Tonya S. Drake
Reg. No. 57,861

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (877) 769-7945

22101798.doc